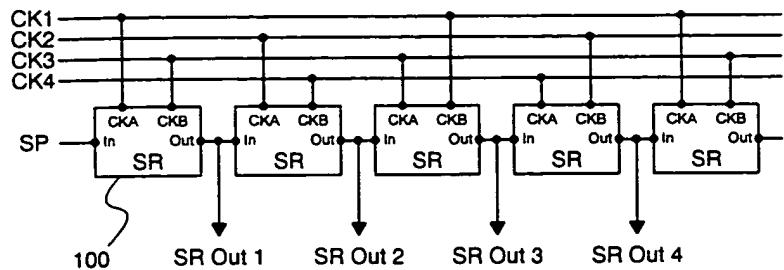
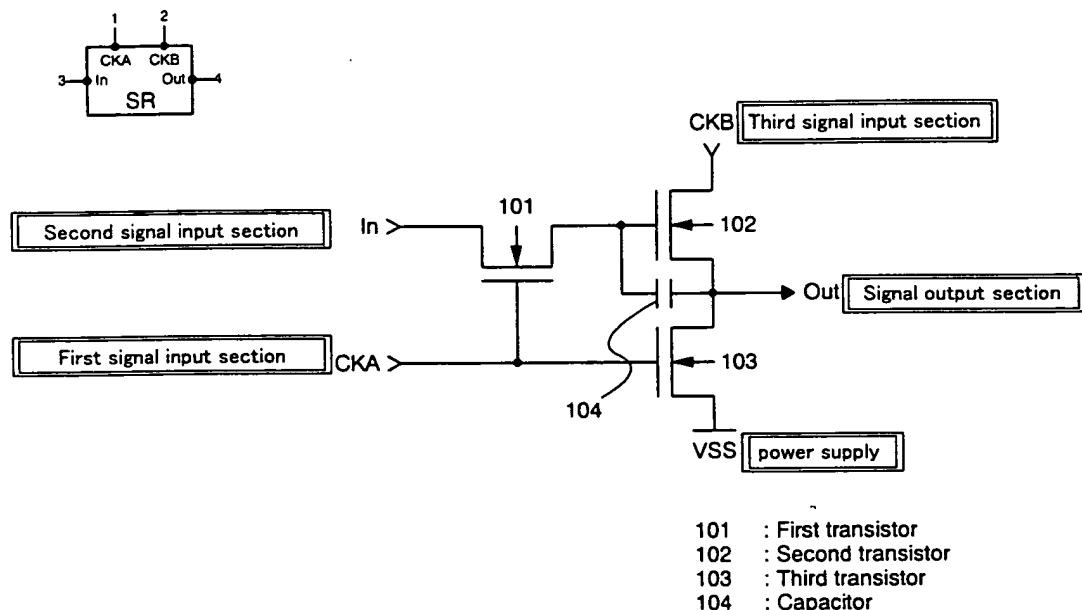


Fig. 1A



CK1 : First clock signal
 CK2 : Second clock signal
 CK3 : Third clock signal
 CK4 : Fourth clock signal
 SP : Start pulse

Fig. 1B



101 : First transistor
 102 : Second transistor
 103 : Third transistor
 104 : Capacitor

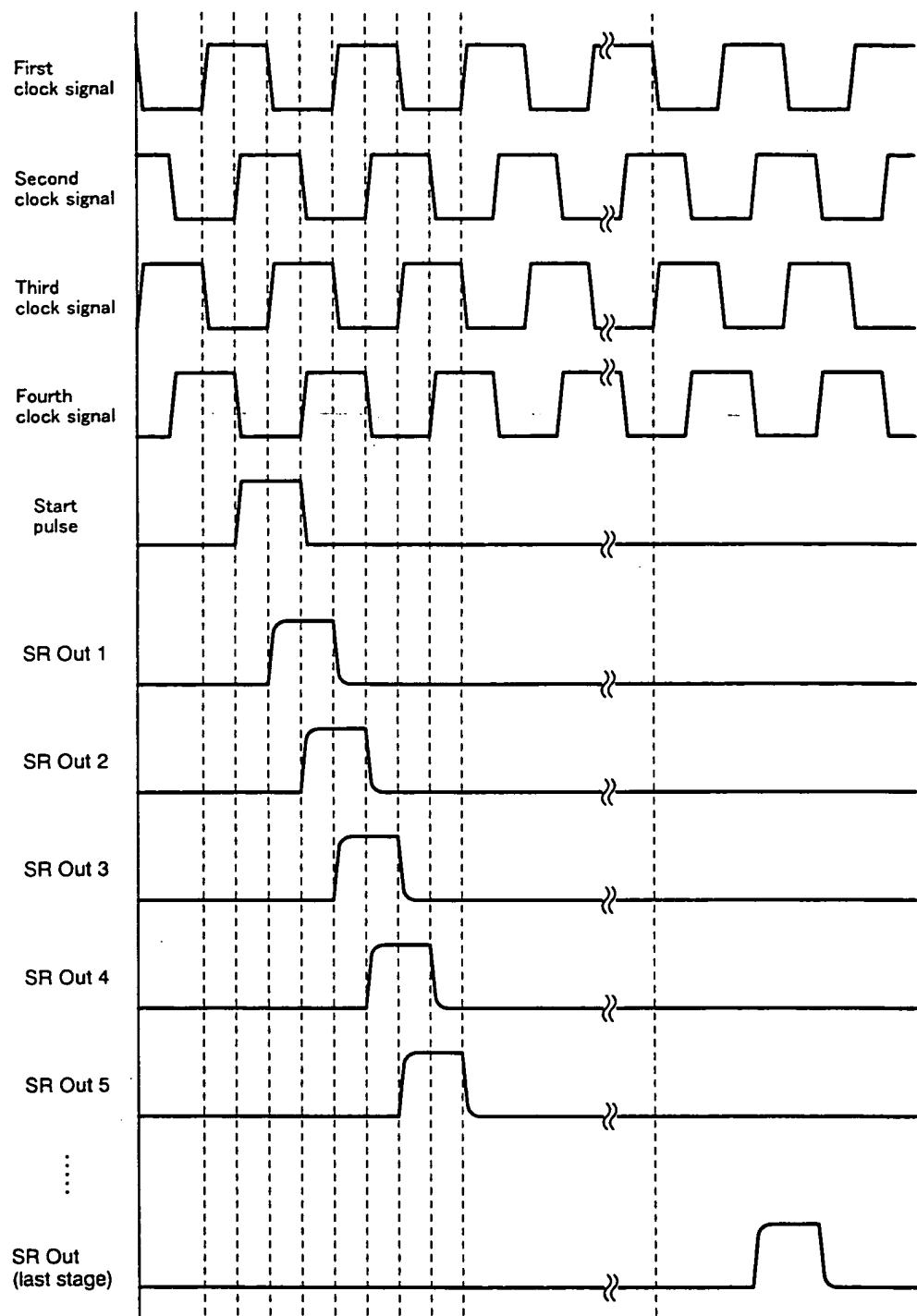
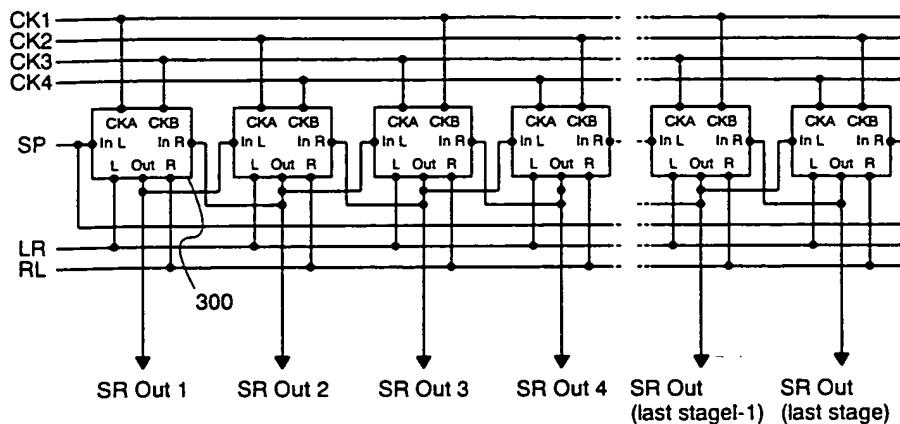


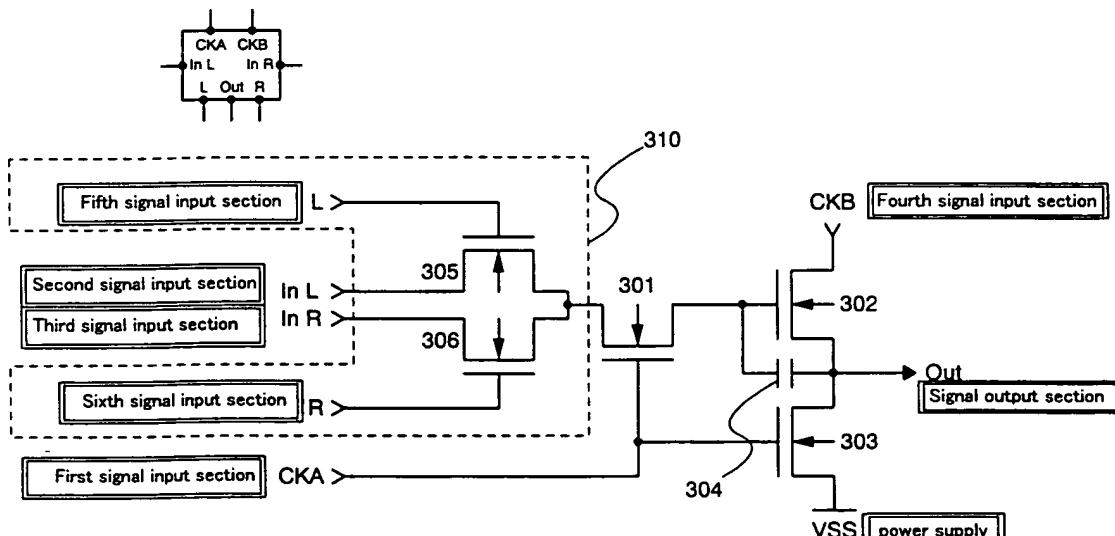
Fig. 2

Fig. 3A



CK1 : First clock signal
 CK2 : Second clock signal
 CK3 : Third clock signal
 CK4 : Fourth clock signal
 SP : Start pulse
 LR : Input change signal
 RL : Inverted input change signal

Fig. 3B



301 : First transistor
 302 : Second transistor
 303 : Third transistor
 304 : Capacitor
 305 : Fourth transistor
 306 : Fifth transistor
 310 : Input change circuit

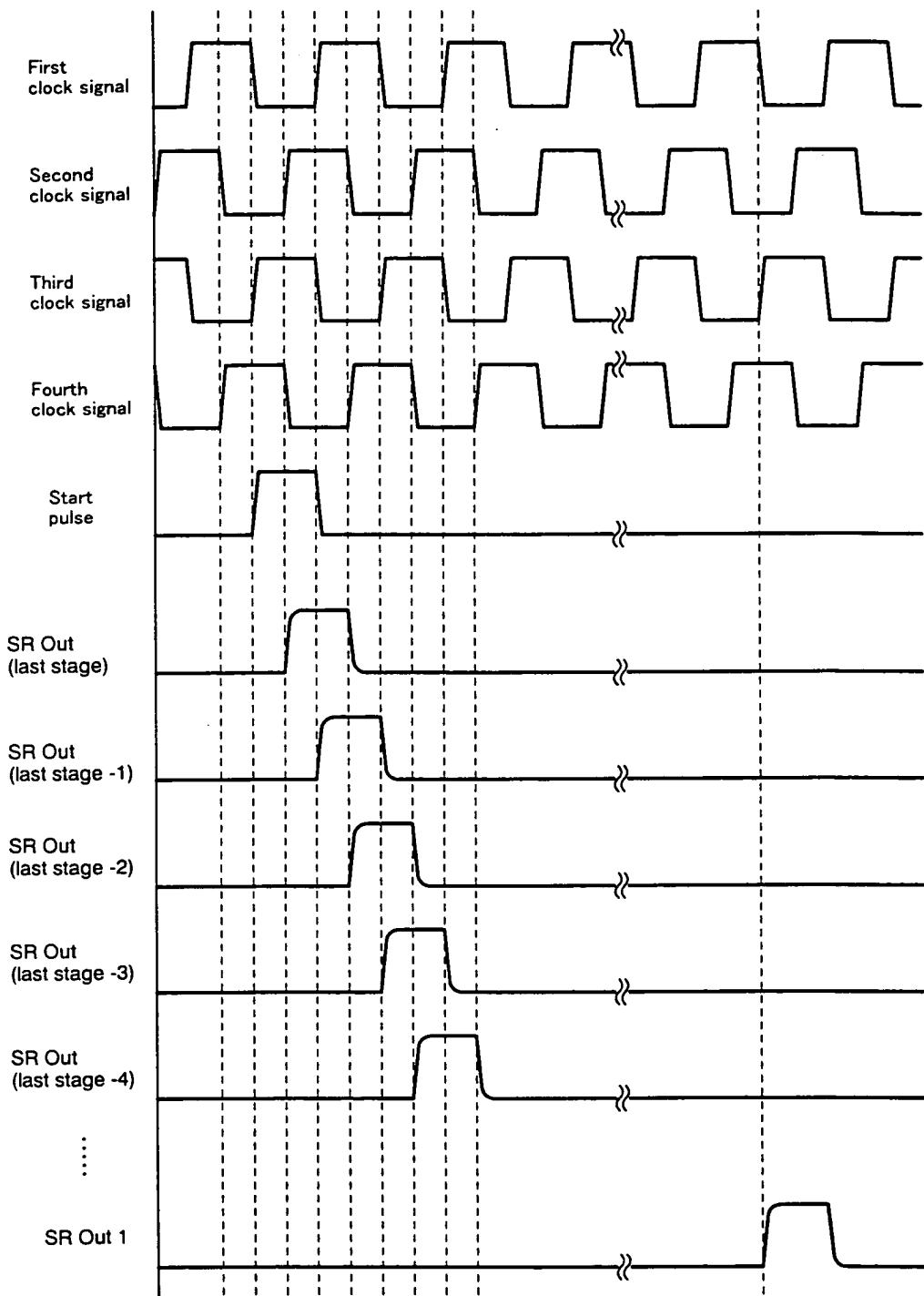


Fig. 4

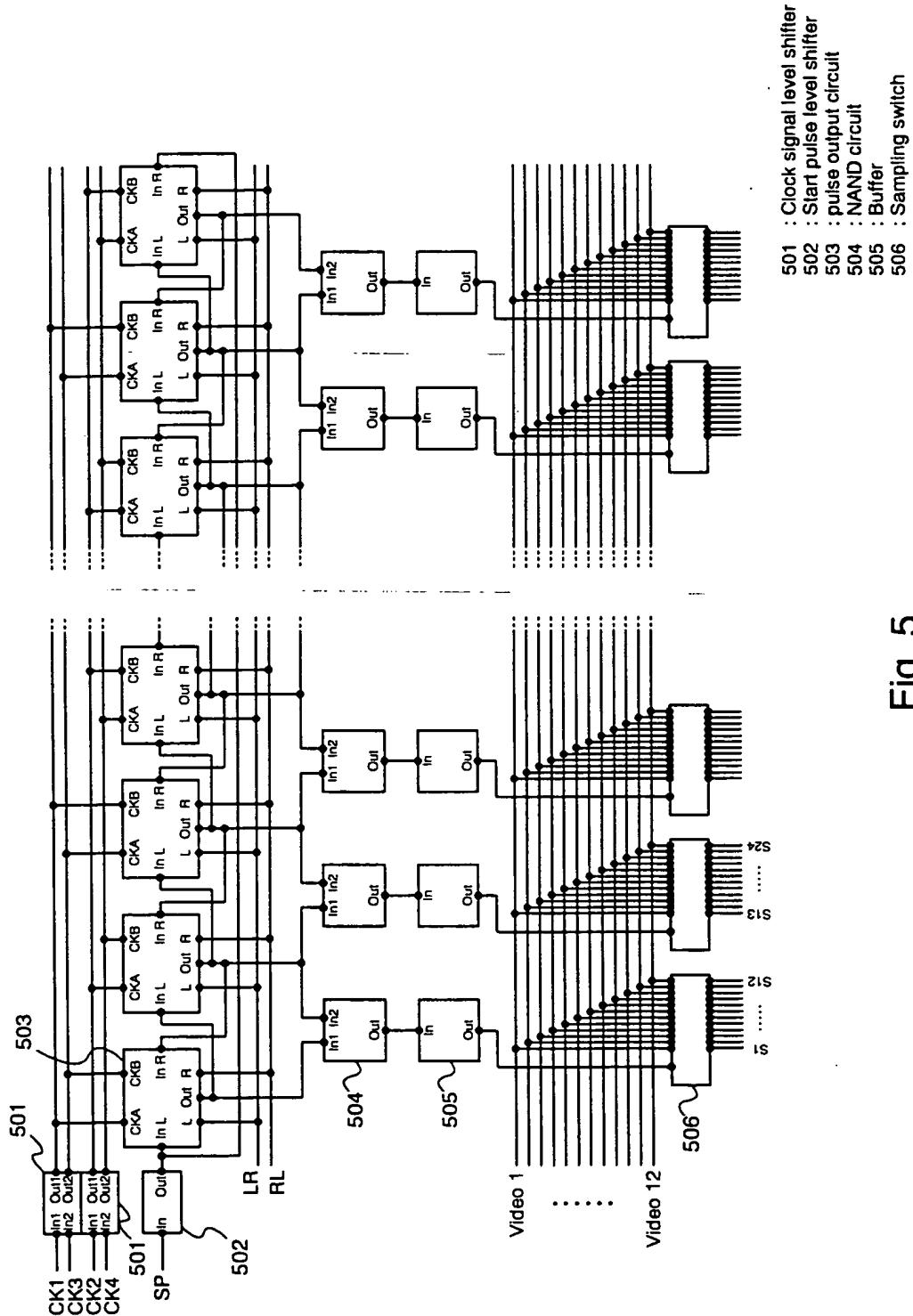


Fig. 5

Fig. 6A

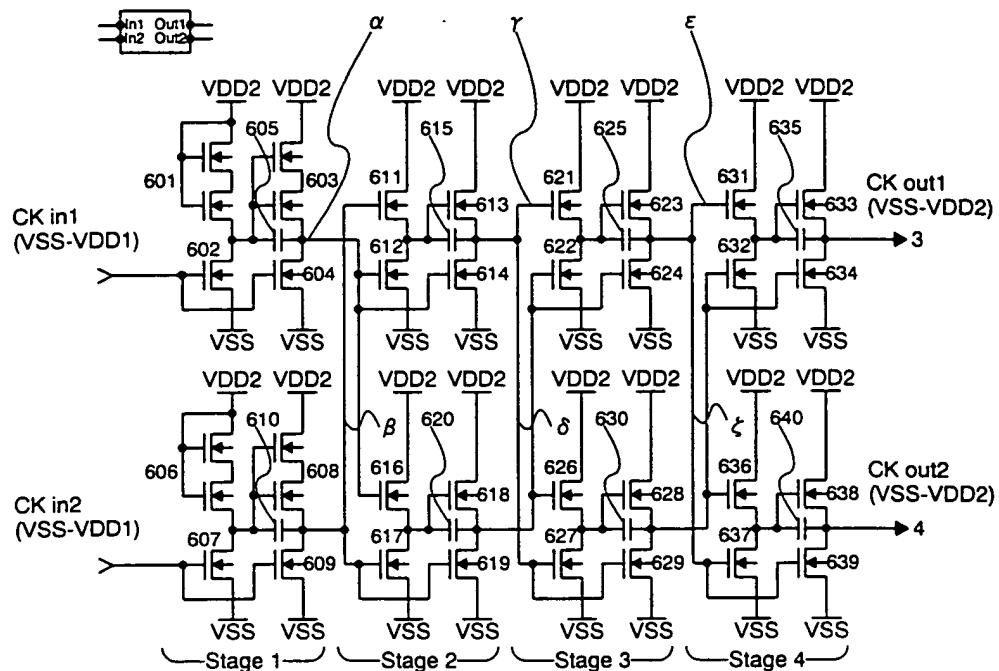


Fig. 6B

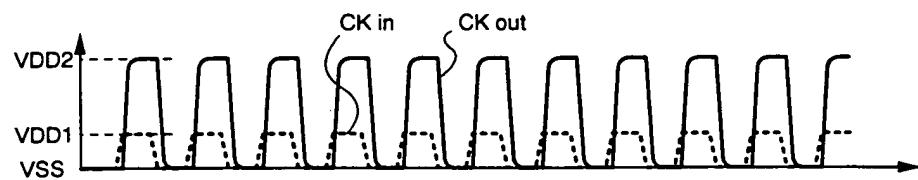


Fig. 6C

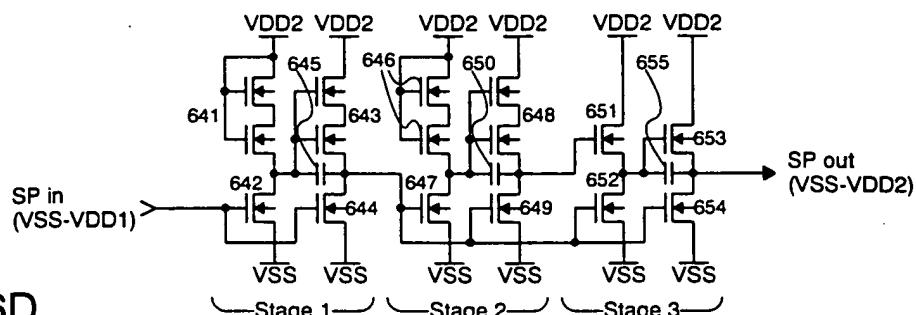
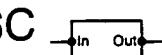


Fig. 6D



Fig. 7A

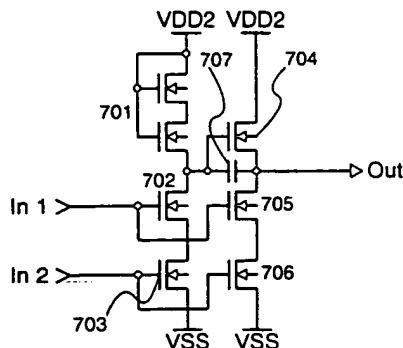
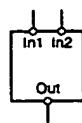


Fig. 7B

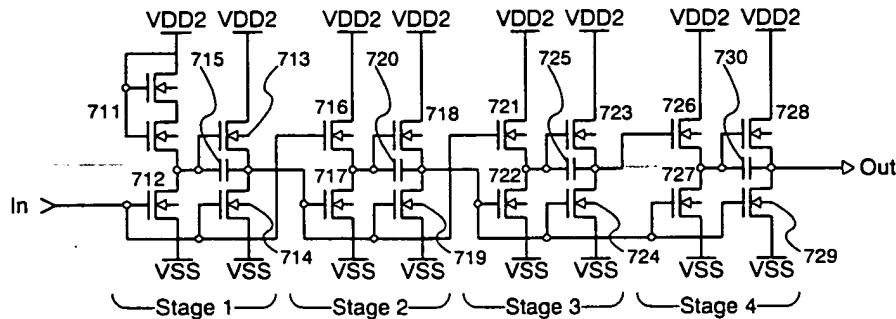
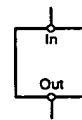
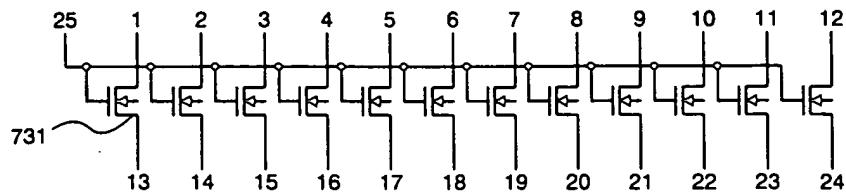
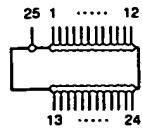


Fig. 7C



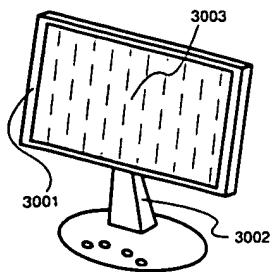


Fig. 8A

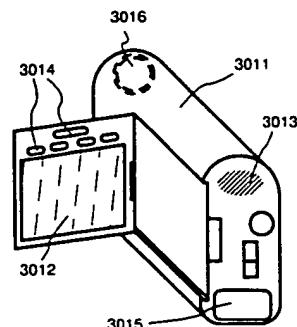


Fig. 8B

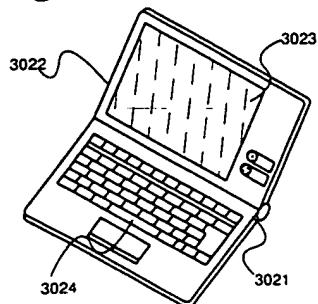


Fig. 8C

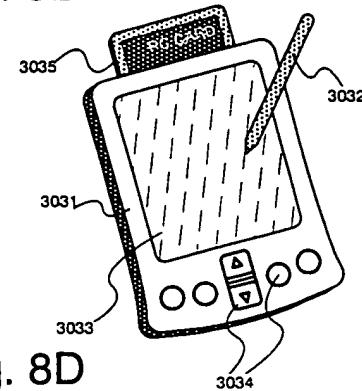


Fig. 8D

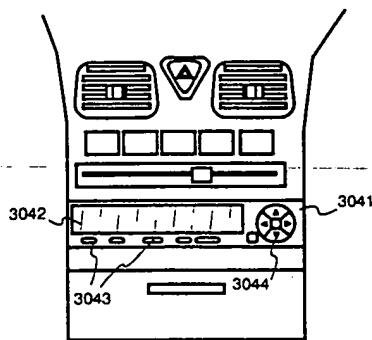


Fig. 8E

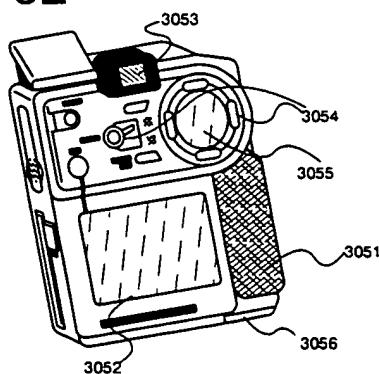


Fig. 8F

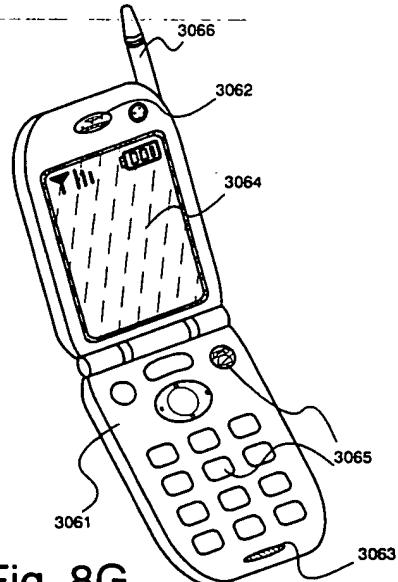


Fig. 8G

Fig. 9A

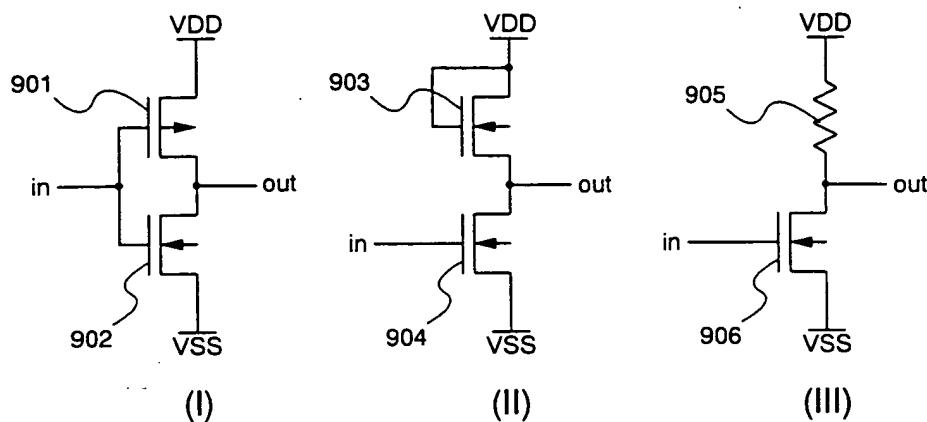


Fig. 9B

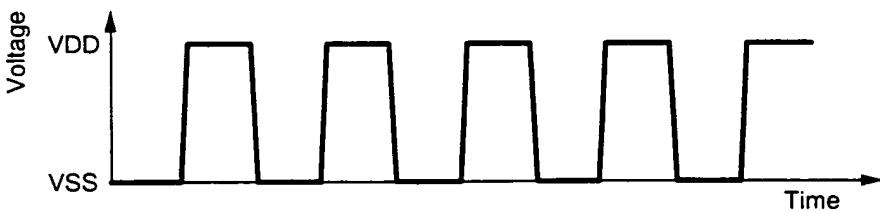


Fig. 9C

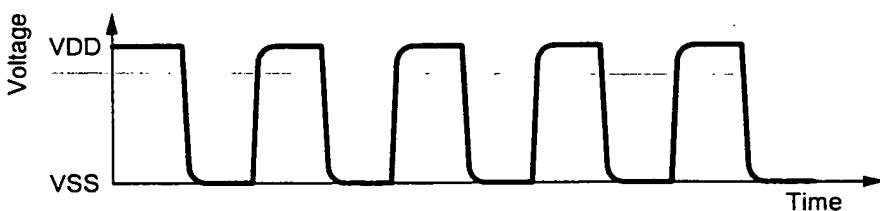


Fig. 9D

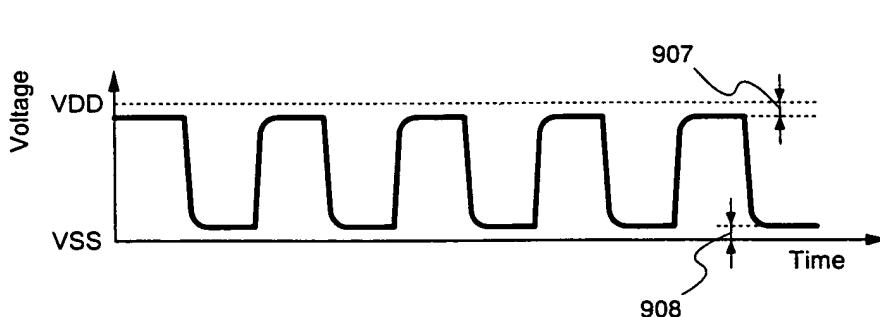
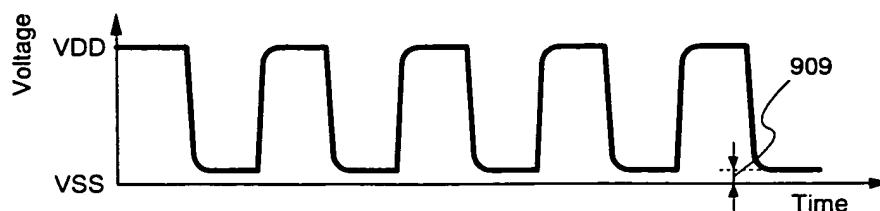


Fig. 9E



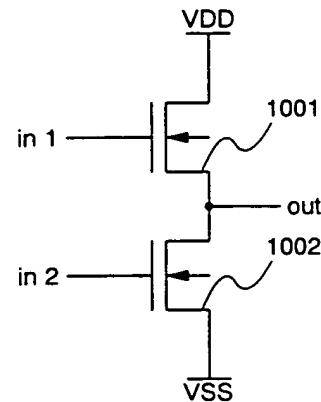


Fig. 10A

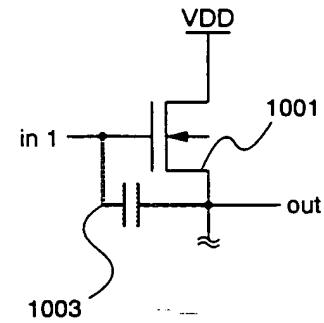


Fig. 10B

Fig. 11A

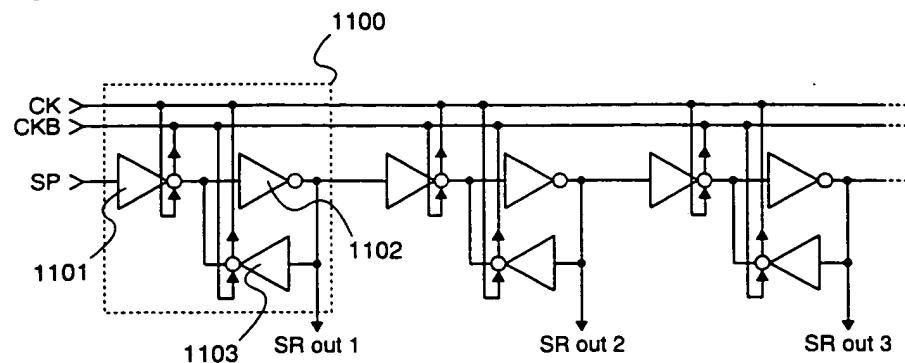


Fig. 11B

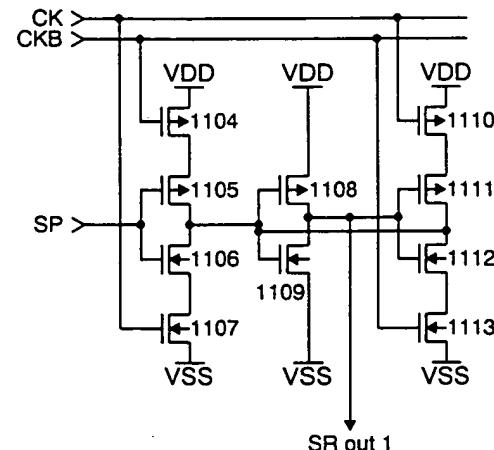
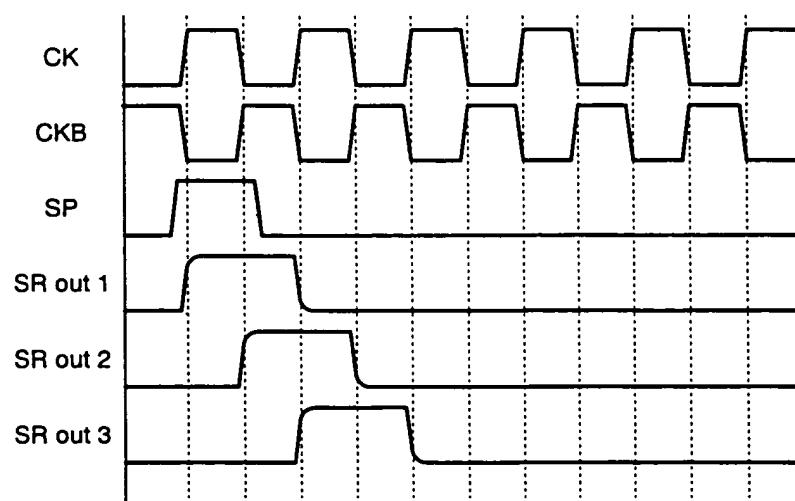


Fig. 11C



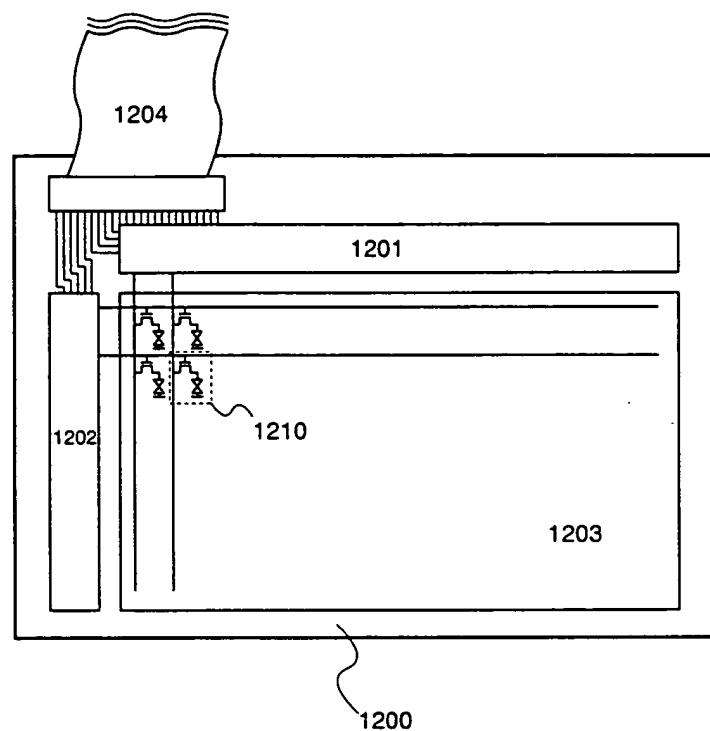
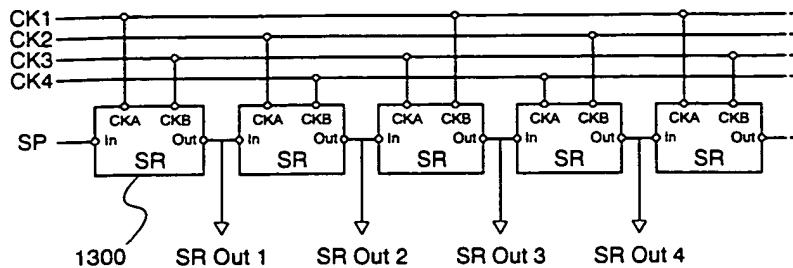


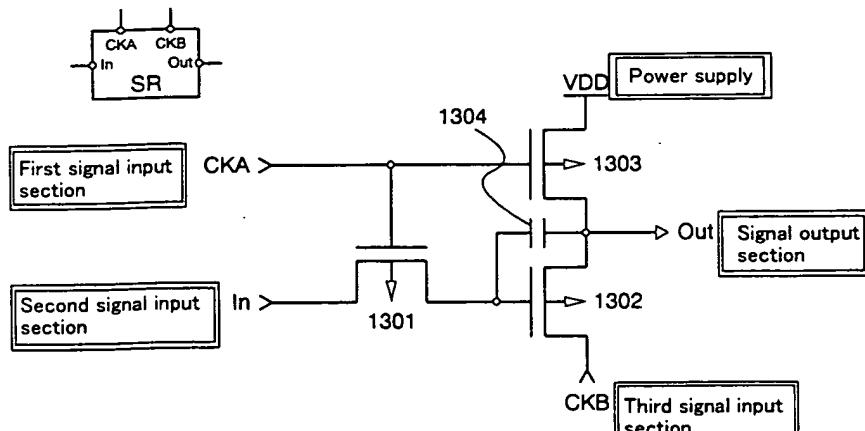
Fig. 12

Fig. 13A



CK1 : First clock signal
 CK2 : Second clock signal
 CK3 : Third clock signal
 CK4 : Fourth clock signal
 SP : Start pulse

Fig. 13B



1301 : First transistor
 1302 : Second transistor
 1303 : Third transistor
 1304 : Capacitor

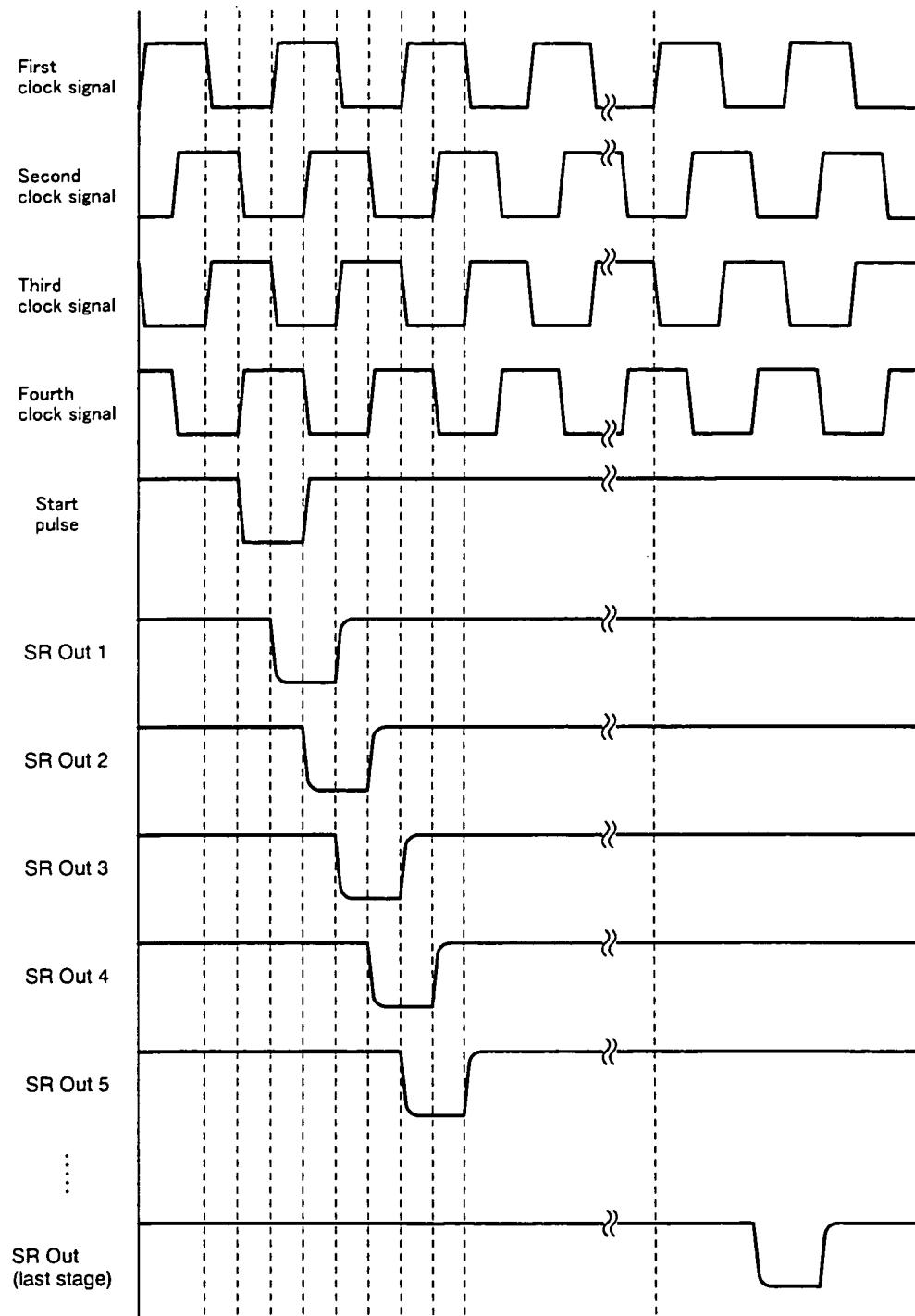


Fig. 14

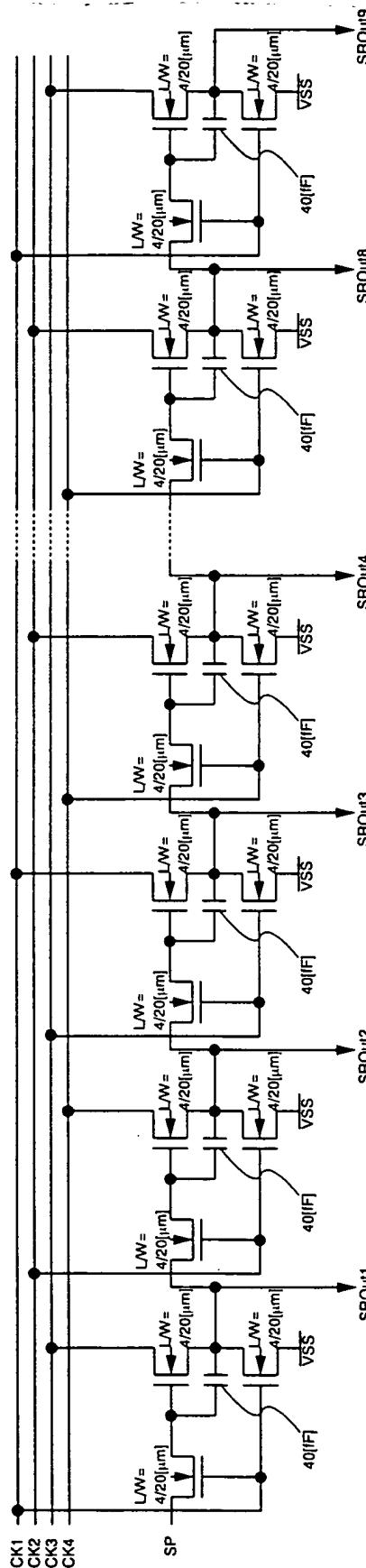


Fig. 15

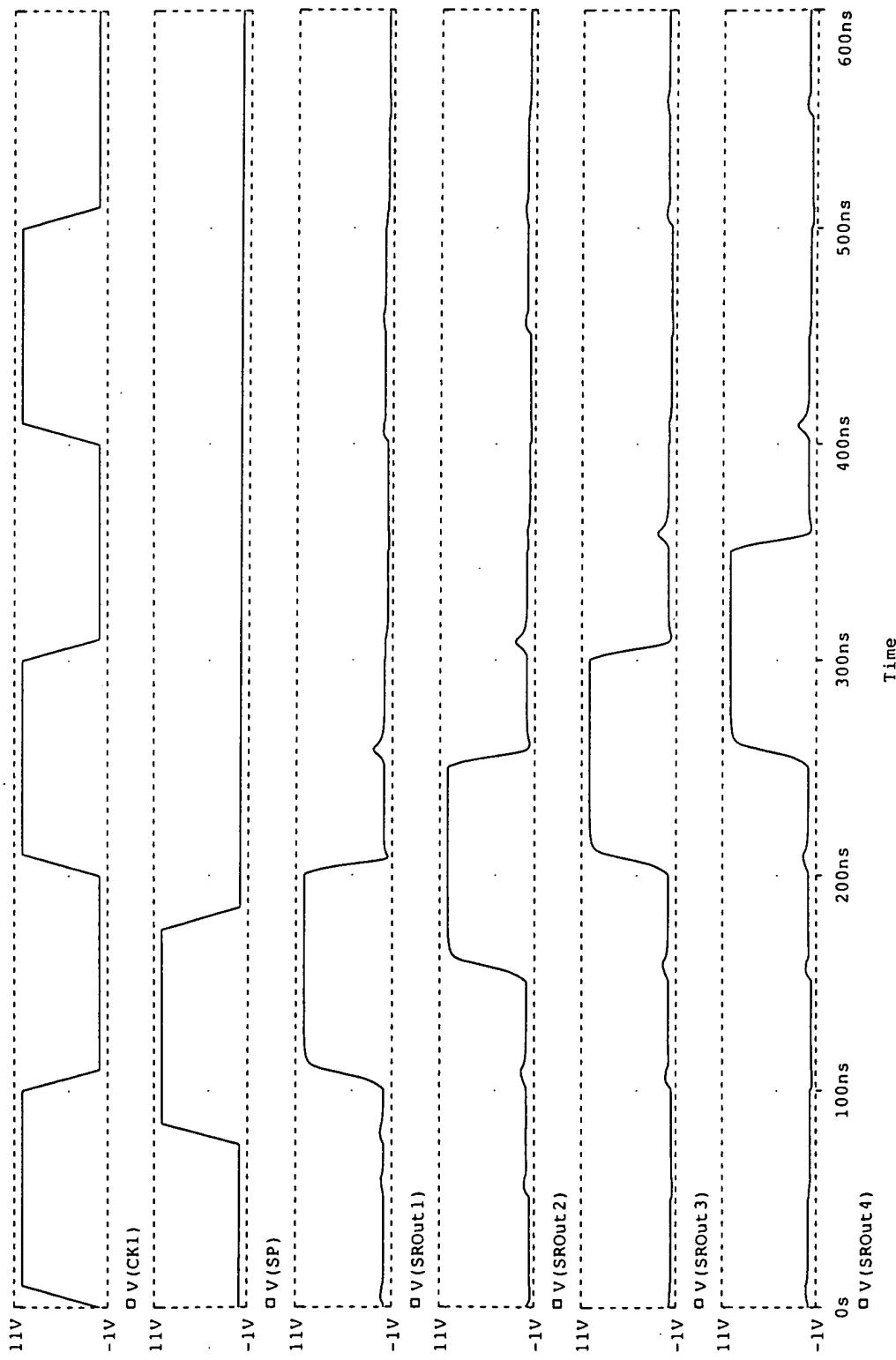


Fig. 16

Fig. 17A

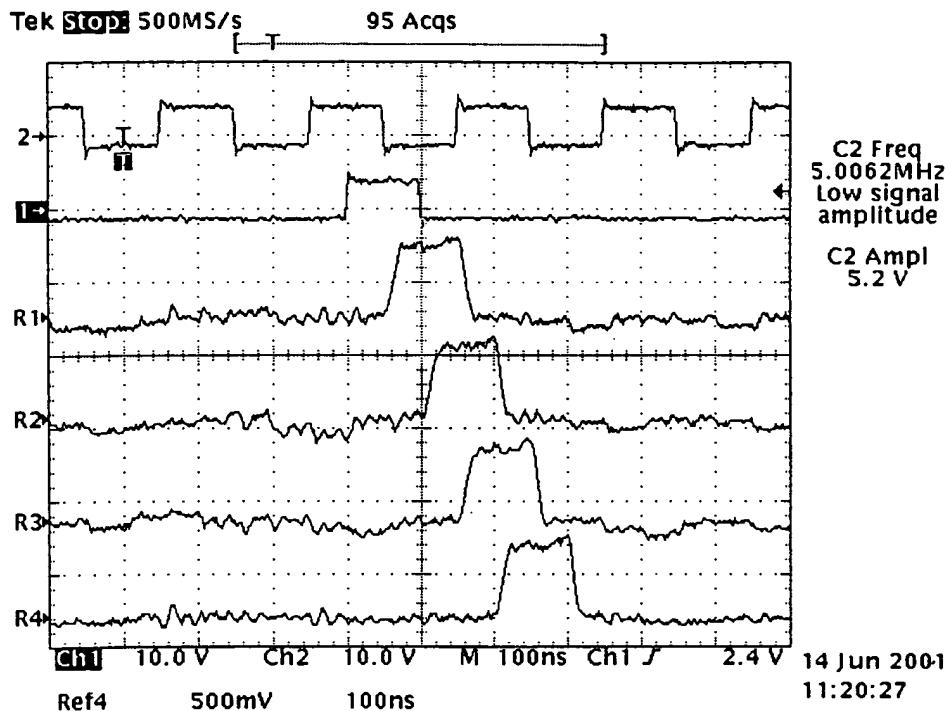


Fig. 17B

